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EXAMINER
FRANKLIN, RICHARD B

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,057	RAPP ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
AU2181

4/14/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 38 have been examined.

Response to Arguments

2. Applicant's arguments filed 17 February 2006 have been fully considered but they are not persuasive.

Applicant amended claim 1 to recite receiving more than one version of firmware, storing the versions of firmware, and downloading a selected version of firmware from the memory. Applicant argued that Carmichael et al. US Patent No. 6,308,311 (hereinafter Carmichael) or any of the other references teach, alone or in combination, all of the limitations of amended claim 1. Applicant argued that only a single configuration can be loaded from the host. However, Examiner submits that Carmichael does teach receiving multiple firmware versions (Carmichael; Col 6 Lines 22 – 35 [default configuration], Col 7 Lines 48 – 53 [new FPGA configuration]), storing the firmware versions in a memory (Carmichael; Figure 7a Item 36c, Col 7 Lines 45 – 53), and based on the configuration mode pins (Carmichael; Figure 3 Items 32c and 32d), selects a firmware version to download and downloads it (Carmichael; Col 6 Lines 11 – 18).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642

F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

As per Applicants arguments with regards to claim 13, Applicant argued that Erickson et al. US Patent Application No. 2003/0177223 (hereinafter Erickson) does not disclose or suggest storing multiple firmware configurations for each processor in memory. However, the Examiner submits that Erickson is not relied upon for storing multiple firmware configurations in memory as Carmichael teaches that limitation. Erickson is relied upon for its teachings of storing and updating firmware for multiple processors. Therefore, Carmichael **in combination with** Erickson teaches all the limitations of claim 13, and Applicant only argued the secondary reference Erickson.

Claim Objections

3. Claims 10, 24, and 32 are objected to because of the following informalities:

a. As per claim 10, it appears that Applicant intended to recite "download a second selected ***one*** of the versions..." (emphasis added) instead of "download a second selected ***on*** of the versions..." (emphasis added) but misspelled the word "one."

b. As per claim 24, it appears that Applicant intended to remove the word "the" from the phrase "download **the** a first firmware code" (emphasis added) but failed to do so.

c. As per claim 32, it appears that Applicant intended to recite "storing **in a** memory a plurality of..." (emphasis added), instead of "storing memory a plurality of..."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 13 – 14, and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 13 recites the limitation "a selected one of the firmware configurations" in Line 16 of the currently amended claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if this limitation is referring to a new "selected one of the firmware configurations" or the "selected one of the firmware configurations" that has been previously been recited in the claim.

The Examiner has interpreted the limitation to refer to a new "selected one of the firmware configurations."

6. Claim 13 recites the limitation "a different one of the firmware configurations" in Line 20 of the currently amended claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if this limitation is

referring to a new "different one of the firmware configurations" or the "different one of the firmware configurations" that has been previously been recited in the claim.

The Examiner has interpreted the limitation to refer to a new "different one of the firmware configurations."

7. Claim 14 recites the limitation "the first configuration" in Lines 4 and 6 of the amended claim. There is insufficient antecedent basis for this limitation in the claim.

The Examiner has interpreted the limitation to refer to the selected of the configurations that is downloaded by the first programmable circuit in claim 13.

8. Claim 24 recites the limitation "the fourth configuration code" in Lines 22 and 23 of the amended claim. There is insufficient antecedent basis for this limitation in the claim.

The Examiner has interpreted the limitation to recite "the fourth firmware code."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1 – 2, 4 – 7, 9 – 12, 16, 20, 23, and 30 – 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Carmichael et al. US Patent No. 6,308,311 (hereinafter Carmichael).

As per claims 1 and 30, Carmichael teaches a programmable circuit to receive multiple versions of firmware that represents a configuration from an external source, store the multiple versions of firmware in a memory (Figure 3 Items 36, Col 7 Lines 45 – 53), and download a selected one of the versions of firmware from the memory (Col 6 Lines 11 – 18, Col 7 Lines 58 – 60).

As per claims 2 and 31, Carmichael teaches that the programmable circuit operates in the configuration corresponding to the downloaded version of firmware after downloading the firmware from the memory (Col 7 Lines 60 – 63).

As per claim 4, Carmichael teaches that the programmable circuit has an external memory (Fig 3 Items 36 or 38).

As per claims 5 and 32, Carmichael teaches a programmable circuit and method to download from a memory storing a plurality of versions of firmware

(Figure 7a Item 36) a first firmware that represents a first configuration (Col 6 Lines 22 – 35), operate in the first configuration, download from the memory a second firmware that represents a second configuration (Col 7 Lines 58 – 60), and operate in the second configuration (Col 7 Lines 40 – 65).

As per claims 6 and 11, Carmichael teaches that the programmable circuit is operable to receive the second firmware version from an external source while operating in the first configuration, and store the second firmware version in the memory while operating in the first configuration (Col 7 Lines 49 – 53), and wherein the second firmware version may only be received when operating in the first configuration (Col 7 Lines 45 – 53).

As per claims 7 and 16, Carmichael teaches a programmable circuit unit comprising a memory (Figure 3 Items 36), a programmable circuit coupled to the memory that can receive multiple versions of firmware that represents corresponding operating configurations of the programmable circuit from an external source (Col 6 Lines 22 – 35, Col 7 Lines 40 – 65), store the firmware in a memory (Figure 3, Col 7 Lines 49 – 53), and download the firmware from the memory (Col 7 Lines 58 – 60).

As per claim 9, Carmichael teaches that the programmable-circuit unit comprises a field-programmable gate array (FPGA) (Figure 3 Item 32).

As per claims 10 and 20, Carmichael teaches a computing machine that includes a processor (Figure 3 Item 34), and a programmable-circuit unit attached to the processor that comprises a memory to store a plurality of versions of firmware, each version respectively representing a corresponding configurations (Figure 3 Items 36 and 38) and can download from the memory a first selected one of the versions of firmware (Col 6 Lines 27 – 35), operate in the first configuration, download from the memory a second selected one of the versions of firmware in response to the processor (Col 7 Lines 58 – 60), and operate in the second configuration (Col 7 Lines 40 – 65).

As per claim 12, Carmichael teaches that the programmable-circuit unit can load the second firmware while operating in the first configuration (Col 7 Lines 58 – 60).

As per claim 23, Carmichael teaches that the computing machine processor can send the selected firmware to the programmable circuit, and that the programmable-circuit can load the different firmware into the memory in response to the processor while operating in the configuration corresponding to the selected one of the firmware versions (Col 7 Lines 49 – 53).

As per claim 33, Carmichael teaches sending the second firmware to the programmable circuit, loading the second firmware into a memory with the programmable circuit while the programmable circuit is operating in the first

configuration (Col 7 Lines 49 – 53), and downloading the second firmware from the memory into the programmable circuit (Col 7 Lines 58 – 60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carmichael et al. US Patent No. 6,308,311 (hereinafter Carmichael) in view of RuDusky US Patent Application Publication No. 2003/0061409 (hereinafter RuDusky).

As per claim 3, Carmichael teaches the programmable circuit with memory as described per claim 1.

Carmichael does not teach that the memory is a non-volatile memory.

RuDusky teaches a programmable circuit that uses a non-volatile electrically erasable and programmable read-only memory (EEPROM) to store configuration information (RuDusky; Paragraph [0049]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Carmichael to include a non-volatile memory to store configuration information because doing

so would allow for the configuration information to remain in the memory even with no power to the system.

As per claim 8, Carmichael teaches the programmable circuit with memory as described per claim 7.

Carmichael does not teach that the memory is an EEPROM.

RuDusky teaches a programmable circuit that uses an EEPROM to store configuration information (RuDusky; Paragraph [0049]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Carmichael to include an EEPROM to store configuration information because doing so would allow for the configuration information to remain in the memory even with no power to the system.

11. Claims 13 – 15, 17 – 18, 24, 27 – 29, 34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carmichael et al. US patent No. 6,308,311 (hereinafter Carmichael) in view of Erickson et al. US Patent Application Publication No. 2003/0177223 (hereinafter Erickson).

As per claim 13, Carmichael teaches a programmable-circuit unit that includes a memory to hold different firmware configurations (Carmichael; Figure 3 Items 36 and 38); and a first programmable circuit coupled to the memory and operable to download a selected one of the configuration from the memory (Carmichael; Col 6 Lines 27 – 35), operate in the configuration corresponding to

the selected firmware configuration, download a different one of the firmware configurations from the memory (Carmichael; Col 7 Lines 58 – 60), and operate in the configuration corresponding to the different firmware configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable circuit coupled to the memory and first programmable circuit that is operable to download a second selected firmware from the memory, operate in the second selected configuration, download a second different firmware from the memory, and operate in the second different configuration.

Erickson teaches a system that has multiple processors (Erickson; Figure 1 Items 112 and 114) or field programmable gate arrays (FPGAs) (Erickson; Paragraph [0013] Lines 14 – 19) running different versions of firmware (Erickson; Figure 1 Items 116 and 118). The firmware running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include multiple FPGAs that run different versions of firmware that is updated because doing so allows firmware to be changed in a system with higher computing power than a single FPGA system.

As per claim 14, Carmichael also teaches receiving the second configuration from an external source while operating in the first configuration

and storing the second configuration in the memory while operating in the first configuration (Carmichael; Col 7 Lines 49 – 53).

As per claim 15, Carmichael also teaches that the programmable-circuit is a FPGA (Carmichael; Figure 3 Item 32).

As per claim 17, Carmichael teaches the computing machine with a processor coupled to a programmable-circuit unit as described per claim 16.

Carmichael does not teach determining whether the firmware is already stored in the memory before sending the firmware to the programmable circuit, and sending the firmware to the programmable circuit only if the firmware is not already stored in the memory.

Erickson teaches determining if a firmware is stored in a memory coupled to the programmable circuit (Erickson; Figure 3 Items 320 – 360) and only sending the firmware to the programmable circuit if the second firmware is not stored in the memory (Erickson; Figure 3 Item 360).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the checking to see if the firmware is already stored in the memory and not sending the firmware if it is already stored because doing so reduces the chance of sending data that has already been sent and thereby wasting processing power on a data transfer that is not needed.

As per claim 18, Carmichael also teaches a configuration registry (Erickson; Figure 1 Items 130 and 140) that stores firmware (Erickson; Figure 1 Item 132, Paragraph [0014]) and indicates that the firmware represents a desired configuration (Erickson; Paragraph [0015]), and that the processor is operable to download the firmware from the configuration registry into the programmable circuit (Erickson; Paragraph [0017] Lines 9 – 13).

As per claim 24, Carmichael teaches a programmable-circuit unit that has a processor (Carmichael; Figure 3 Item 34); a memory to hold different firmware configurations (Carmichael; Figure 3 Items 36 and 38); and a first programmable circuit coupled to the memory and operable to download a first configuration from the memory (Carmichael; Col 6 Lines 27 – 35), operate in the first configuration, download a second configuration from the memory in response to the processor (Carmichael; Col 7 Lines 58 – 60), and operate in the second configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable circuit coupled to the memory and the first programmable circuit that is operable to download a third firmware from the memory, operate in the third configuration, download a fourth firmware from the memory in response to the processor, and operate in the fourth configuration.

Erickson teaches a system that has multiple processors (Erickson; Figure 1 Items 112 and 114) or FPGAs (Erickson; Paragraph [0013] Lines 14 – 19) running different versions of firmware (Erickson; Figure 1 Items 116 and 118).

The firmware running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include multiple FPGAs that run different versions of firmware that is updated because doing so allows firmware to be changed in a system with higher computing power than a single FPGA system.

As per claim 27, Carmichael also teaches receiving the second configuration from an external source and storing it in memory while operating in the first configuration (Carmichael; Col 7 Lines 49 – 53).

As per claim 28, Erickson also teaches a separate memory unit to hold firmware information for each processor (Erickson; Figure 1 Items 120 and 122).

As per claim 29, Carmichael in combination with Erickson obviously teaches that the separate memories are disposed on separate integrated circuits because putting memories on different integrated circuits would be an obvious engineering choice (See *In re Larson*, 340 F.2d 965, 967, 144 USPQ 347, 349 (CCPA 1965); *In re Wolfe*, 251 F.2d 854, 855, 116 USPQ 443, 444 (CCPA 1958)).

As per claim 34, Carmichael teaches the method as described per claim 32 and loading the second firmware into the memory with the programmable circuit while operating in the first configuration (Carmichael; Col 7 Lines 58 – 60) and downloading the second firmware from the memory into the programmable circuit (Carmichael; Col 7 Lines 40 – 65)

Carmichael does not teach determining if the second firmware is stored in a memory coupled to the programmable circuit and sending the second firmware to the programmable circuit only if the second firmware is not stored in the memory.

Erickson teaches determining if the second firmware is stored in a memory coupled to the programmable circuit (Erickson; Figure 3 Items 320 – 360) and only sending the second firmware to the programmable circuit if the second firmware is not stored in the memory (Erickson; Figure 3 Item 360).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the checking to see if the firmware is already stored in the memory and not sending the firmware if it is already stored because doing so reduces the chance of sending data that has already been sent and thereby and wasting processing power on a data transfer that is not needed.

As per claim 36, Carmichael teaches a first programmable circuit coupled to a memory that stores a plurality of firmware codes (Carmichael; Figure 3 Items 36 and 38) and operable to download a first configuration from the memory

(Carmichael; Col 6 Lines 27 – 35), operate in the first configuration, download a third configuration from the memory (Carmichael; Col 7 Lines 58 – 60), and operate in the third configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable circuit coupled to the memory and the first programmable circuit that is operable to download a second firmware from the memory, operate in the second configuration, download a fourth firmware from the memory, and operate in the fourth configuration.

Erickson teaches a system that has multiple processors (Erickson; Figure 1 Items 112 and 114) or FPGAs (Erickson; Paragraph [0013] Lines 14 – 19) running different versions of firmware (Erickson; Figure 1 Items 116 and 118). The firmware running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include multiple FPGAs that run different versions of firmware that is updated because doing so allows for firmware to be changed in a system with higher computing power than a single FPGA system.

12. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carmichael et al. US Patent No. 6,308,311 (hereinafter Carmichael) in view of Hartmann US Patent No. 6,096,091 (hereinafter Hartmann).

As per claim 19, Carmichael teaches the computing machine with a processor coupled to a programmable-circuit unit as described per claim 16.

Carmichael does not teach that the programmable-circuit unit comprises a pipeline unit, and that the programmable circuit includes a hardwired pipeline that can operate on data.

Hartmann teaches the use of a reconfigurable programmable circuit unit that includes a pipeline unit (Hartmann; Figure 2, Col 2 Lines 32 – 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include a pipeline unit because doing so would speed up data processing of the system.

13. Claims 21 – 22, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carmichael et al. US Patent No. 6,308,311 (hereinafter Carmichael) in view of Moore US Patent No. 6,893 873 (hereinafter Moore).

As per claim 21, Carmichael teaches the computing machine as described per claim 20.

Carmichael does not teach that the processor has a first test port, the programmable circuit has a second test port coupled to the first test port, and the processor is able to load the selected one of the firmware into memory via the first and second test ports.

Moore teaches a programmable circuit with a test port (Moore; Figures 2A – 2C Item 206). The programmable circuit performs a self-test (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31) and can send the result to a processor through the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded

into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the test ports and data transfer through the test ports because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

As per claim 22, Moore also teaches that the processor comprises a first test port, the programmable-circuit unit comprises a second test port that is coupled to the first test port (Moore; Figures 2A – 2C Item 206), the programmable circuit can perform a self-test and send self-test data to the processor via the first and second test ports (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31), and firmware is then loaded into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

As per claim 35, Carmichael teaches the method as described per claim 32.

Carmichael does not teach that operating the programmable circuit in the first configuration comprises testing the programmable circuit, and downloading the second firmware comprises downloading the second firmware only if the programmable circuit passes testing.

Moore teaches a programmable circuit with a test port (Moore; Figures 2A – 2C Item 206). The programmable circuit performs a self-test (Moore; Figure 3

Item 308, Col 5 Lines 28 – 31) and can send the result to a processor through the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the test ports, self-test, and data transfer through the test ports only if a certain test result was discovered because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

14. Claims 25 – 26, and 37 – 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carmichael et al. US Patent No. 6,308,311 (hereinafter Carmichael) in view of Erickson et al. US Patent Application Publication No. 2003/0177223 (hereinafter Erickson) as applied to claims 13 – 15, 17 – 18, 24, 27 – 27, 34, and 36 above, and further in view of Moore US Patent No. 6,893,873 (hereinafter Moore).

As per claim 25, Carmichael in combination with Erickson teaches a computing machine with multiple programmable circuits as described per claim 24.

Carmichael in combination with Erickson does not teach that the processor has a first test port, the programmable circuit has a second test port coupled to the first test port, and the processor is able to load the first and third firmware into memory via the first and second test ports.

Moore teaches a programmable circuit with a test port (Moore; Figures 2A – 2C Item 206). The programmable circuit performs a self-test (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31) and can send the result to a processor through the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael in combination with Erickson to include the test ports, self-test, and data transfer through the test ports only if a certain test result was discovered because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

As per claim 26, Moore also teaches the first and second programmable circuits to perform self-tests (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31) and provide the self-test data to the processor via the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67), and then each programmable circuit loads a different firmware if the self-test data indicate a predetermined result of the self-tests (Moore; Figure 2C, Col 6 Lines 4 – 13).

As per claim 37, Carmichael in combination with Erickson teaches a method including multiple programmable circuits as described per claim 36.

Carmichael in combination with Erickson does not teach wherein downloading the first and second firmware comprises downloading the first and second firmware into the first and second programmable circuits via a test port.

Moore teaches a programmable circuit with a test port (Moore; Figures 2A – 2C Item 206). The programmable circuit performs a self-test (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31) and can send the result to a processor through the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael in combination with Erickson to include the loading of firmware though test ports because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

As per claim 38, Moore also teaches testing the first and second programmable circuits (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31), and wherein loading the firmware into the programmable circuits comprises loading the firmware only if the testing indicates that the programmable circuit is functioning as desired (Moore; Figure 2c, Col 6 Lines 4 – 13).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard Franklin
Patent Examiner
Art Unit 2181

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4/14/2006